IN THE CLAIMS:

Claim 1. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, and ~~independently of each other~~ when detecting that a power is supply switch on; ~~and~~

a main reset signal generator including a plurality of pulse generators for respectively generating ~~a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least~~ pulses on the basis of a translation edge for a corresponding one ~~from any~~ of said sub power-on reset signals ; and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal.

Claim 2. (Canceled)

Claim 3. (Canceled)

Claim 4. (Previously amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a sub power-on reset signal;

a reset terminal for receiving an external power-on reset signal; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal,

wherein said main reset signal generator comprises

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signal and said external power-on reset signal, and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 5. (Canceled)

Claim 6. (Currently Amended) A semiconductor integrated circuit ~~according to claim 5, wherein said main reset signal generator comprises~~ comprising:

a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different for each other, when detecting that a power supply is switched on;

a reset terminal for receiving an external power-on rest signal; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-reset signals and said external power-on reset signal,

wherein said main rest signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signals and said external power-on reset signal; , and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 7. (Currently amended) A method of initializing a semiconductor integrated circuit comprising the steps of:

generating ~~a plurality of pulse signals as power-on reset signals according to~~ a plurality of sub power-on reset signals at timings different from each other, ~~and independently of each other~~, when detecting that a power supply is switched on;

respectively generating pulses on the basis of a transition edge for a corresponding ~~at least~~ one of said ~~pulse~~ sub power-on reset signals ~~including a rectangular pulse~~; and

~~initializing an internal circuit according to at least one from any of~~ synthesizing the pulses to generate said main power-on reset ~~signals~~ signal.

Claim 8. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of sub reset signal generators, including transistors having threshold values, for generating a plurality of sub power-on reset signals on basis of the respective threshold values of each of the transistors, ~~and independently of each other~~ when detecting that a power supply is switched on; and

a main reset signal generator including a plurality of pulse generators for respectively generating ~~a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least~~ pulse on the basis of a transition edge for a corresponding one of said sub power-on reset signals ; and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal.

Claim 9. (Currently amended) A semiconductor integrated circuit comprising:

a first sub reset signal generator, including a first transistor having a first threshold value, for generating a first sub power-on reset signal on basis of the first threshold value when detecting that a power supply is switched on;

a second sub reset signal generator, including a second transistor having a second threshold value, for generating a second sub power-on reset signal on basis of the second threshold value, ~~independently of the first sub reset signal generator~~ when detecting that a power supply is switched on; and

a main reset signal generator including a plurality of pulse generators for respectively generating ~~a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least~~ pulses on the basis of a transition edge for a corresponding one of the first sub power-on reset signal and the second sub power-on reset signal ;and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal.

Claim 10. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, ~~and independently of each other~~ when detecting that a power supply is switched on;

a plurality of pulse generators for generating pulses on the basis of the plurality of sub power-on reset signals, respectively, at least one of said pulses being a rectangular pulse; and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal.

Claim 11. (Currently amended) A method of initializing a semiconductor integrated circuit having a plurality of sub reset signal generators including transistors having threshold values, the method comprising the steps of:

generating a plurality of sub power-on reset signals, each according to respective threshold values of each of the transistors, ~~and independently of each other~~ when detecting that a power supply is switched on;

respectively generating ~~a plurality of pulse signals as power-on reset signals, according to the plurality of~~ pluses on the basis of a transition edge for a corresponding one of said sub power-on reset signals ~~generated at timings different from each other~~, at least one of said ~~pulse signals~~ pulses including a rectangular pulse; and

~~initializing an internal circuit according to at least one of~~ synthesizing the pulses to generate said main power-on reset signals.

Claim 12. (Canceled)

Claim 13. (Canceled)

Claim 14. (Currently amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a sub power-on reset signal;

a reset terminal for receiving an external power-on reset signal supplied from the exterior of the semiconductor integrated circuit; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal,

wherein said main reset signal generator comprises

a plurality of pulse generators, wherein each pulse generator generates a

respective pulse on the basis of a respective transition edge which corresponds to one of said sub power-on reset signal and said external power-on reset signal;, and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 15. (Canceled)

Claim 16. (Original) A semiconductor integrated circuit ~~according to claim 15, wherein said main reset signal generator comprises~~ comprising:

a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, when detecting that a power supply is switched on:

a reset terminal for receiving a external power-on reset signal supplied from the exterior of the semiconductor integrated circuit; and

a main reset signal generator for generating a rectangular pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on resets signals and said external power-on reset signal,

wherein said main reset signal generators comprises

a plurality of pulse generators, wherein each pulse generator generates a respective pulse on the basis of a respective transition edge which corresponds to one of said sub power-on reset signal and said external power-on reset signal;, and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 17. (Canceled)

Claim 18. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, ~~and independently of each other;~~ when detecting that a power supply is switched on; and

a main reset signal generator including a plurality of pulse generators for respectively generating ~~a main power-on reset signal to initialize an internal circuit, according to at least~~ pulses on the basis of a transition edge for a corresponding one of said ~~plurality of~~ sub power-on reset signals~~,~~ ; and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal, wherein

said main reset signal generator generates said main power-on reset signal having pulses respectively corresponding to each of said sub power-on reset signals, when threshold values of transistors formed in said semiconductor integrated circuit are typical values.

Claim 19. (Canceled)

Claim 20. (Currently amended) A method of initializing a semiconductor integrated circuit having a plurality of sub reset signal generators including transistors having threshold values, the method comprising the steps of:

generating a plurality of sub power-on reset signals, each according to respective threshold values of each of the transistors, ~~and independently of each other~~ when detecting that a power supply is switched on;

respectively generating ~~a plurality of pulse signals as power-on reset signals, according to the plurality of~~ pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signals ~~generated at timings different from each other~~,

said ~~power-on reset signals having~~ pulses not overlapping each other when threshold values of transistors formed in said semiconductor integrated circuit are typical values; and

~~initializing an internal circuit according to at least one of the pulses of~~ synthesizing the pulses to generate said main power-on reset ~~signals~~ signal.

Claim 21. (New) A semiconductor integrated circuit comprising:

a first sub reset signal generator for generating a first sub power-on reset signal when detecting that a power supply is switched on;

a second sub reset signal generator for generating a second sub power-on reset signal when detecting that a power supply is switched on;

a main reset signal generator including a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of the first sub power-on reset signal and the second power–on reset signal; and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal.